**IN THE UNITED STATES DISTRICT COURT**
**FOR THE DISTRICT OF MASSACHUSETTS**

| | |
|---|---|
| SINGULAR COMPUTING LLC,<br><br>Plaintiff,<br><br>v.<br><br>GOOGLE LLC,<br><br>Defendant. | C.A. No. 1:19-cv-12551-FDS<br><br>Hon. F. Dennis Saylor IV |

**DECLARATION OF MIRIAM LEESER, PH.D. IN SUPPORT OF DEFENDANT GOOGLE LLC'S OPPOSITION TO PLAINTIFF SINGULAR COMPUTING LLC'S MOTION FOR PARTIAL SUMMARY JUDGMENT OF VALIDITY BASED UPON IPR ESTOPPEL UNDER 35 U.S.C. § 315(e)(2)**

I, Miriam Leeser, hereby declare as follows:

1. I am a professor of Electrical and Computer Engineering at the Northeastern University College of Engineering, where I have been since 1996. I have personal knowledge of the facts stated herein and could competently testify to them under oath.

2. I have been retained by Google to evaluate and offer my opinions regarding whether claim 53 of U.S. Patent No. 8,407,273 and claim 7 of U.S. Patent No. 9,218,156 (the "Asserted Claims") are invalid as anticipated and/or obvious in light of my work related to the Variable-Precision Floating Point Library, otherwise known as "VFLOAT." I expect to finalize a related report summarizing my opinions by the Court-ordered deadline (which I understand to be, currently, December 22, 2022).

3. VFLOAT is a library (or set) of parameterizable code modules for performing arithmetic operations on floating-point numbers of various formats using reconfigurable hardware, namely field programmable gate arrays (FPGAs). What that means is that a designer using VFLOAT could quickly deploy, onto FPGA hardware, circuits containing multiplication units and other floating-point arithmetic modules that operate on a variety of customizable floating-point number formats. The designer simply selects the floating-point format they wish to use by specifying bitwidths for the exponent and fraction; the code in the library could then create the corresponding VFLOAT arithmetic modules for implementation on FPGAs.

4. VFLOAT was developed by myself and others in the 2000-2002 timeframe at the Reconfigurable Computing Laboratory (RCL) at Northeastern University (back when it was known as the Rapid Prototyping Laboratory or RPL), the group that I have led since 1996.

5. The genesis of VFLOAT can be traced to my work for Los Alamos National Laboratory (LANL) in approximately 1999-2002. I began working for LANL on a sub-contract

received by Northeastern University, which was funded by a grant from the U.S. Defense Advanced Research Projects Agency (DARPA). The formal title of the sub-contract was "Acceleration of Scene Classification and Spectral Unmixing with Reconfigurable Computing." My general objective for this sub-contract with LANL was to explore ways to use FPGAs to quickly analyze large volumes of satellite data that LANL received and needed to process, and more specifically to accelerate their ability to analyze this data compared to existing techniques.

6. VFLOAT became the deliverable for our work for LANL. Under my guidance, a master's student named Pavle Belanović developed a library of hardware modules for performing variable-precision floating-point arithmetic on FPGAs, which we later named VFLOAT—the "FLOAT" signifying that the modules in the library were designed to perform arithmetic operations using floating-point numbers and the "V" signifying that the modules were *variable* in that they used custom, user-defined floating-point number formats (that is, floating-point formats that could have different numbers of exponent and fraction bits fraction bits as compared to the IEEE standard single-precision format).

7. The initial version of VFLOAT was developed specifically for our work for LANL, and LANL directed us to open-source (*i.e.*, non-classified) data sets to validate the use of VFLOAT for their specific application (analyzing satellite imagery and other data).

8. I personally traveled to New Mexico several times during the course of our work with LANL's Space and Remote Sensing Sciences Group to discuss and present our work related to VFLOAT to the officials there, and Mr. Belanović accompanied me on at least one occasion.

9. The original code comprising VFLOAT, along with documentation describing the purpose and functionality of the library is accessible at https://coe.northeastern.edu/Research/rcl/projects/floatingpoint/index.html.

10. The VFLOAT library included parameterizable modules that were designed to be—and were—used in combination, kind of like Lego building blocks, for programming FPGA circuits. For example, 2 *denorm*, 1 *fp_add*, and 1 *rnd_norm* were assembled to create a complete adder circuit, and 2 *denorm*, 1 *fp_mul*, and 1 *rnd_norm* would be assembled to create a complete multiplier circuit.

11. FPGAs are a form of reconfigurable hardware whose structure or architecture can be specified by a designer after manufacturing, typically using a Hardware Description Language (HDL). In the case of VFLOAT, we programmed the design of the various hardware modules in VHDL (VHSIC Hardware Description Language). When mapped to FPGA hardware, VFLOAT modules define circuits that are structured and behave as specified by the VHDL code.

12. In addition to developing the VFLOAT library and making it available via our website, we used the code to implement various arithmetic circuits on FPGA hardware in order to validate and further our work, including determining how many adders or multipliers could be deployed within a particular FPGA, depending on the selected floating-point format.

13. The specific FPGA hardware we used was the first-generation "WILDSTAR" reconfigurable computing engine, which was commercially available from Annapolis Microsystems, a seller of computing hardware based in Annapolis, Maryland. The WILDSTAR reconfigurable computing engine was first announced by Annapolis Microsystems in mid-1999 and had been available commercially for a year or two by the time of our work.

14. The particular form factor of the WILDSTAR reconfigurable computing engine that we used in our work was the PCI board. Shown below is an exemplary photo of the WILDSTAR PCI board. We used the board's PCI bus interface, which can be seen in the below photo, to connect it to a host workstation.

15. The WILDSTAR board we used contained 3 Xilinx Virtex XCV1000 FPGAs. Each of the XCV1000 FPGAs contained the equivalent of just over 1,000,000 system gates for a total of 6,144 CLBs ("configurable logic blocks"), with each CLB comprising 2 "slices" for a total of 12,288 slices per FPGA. The WILDSTAR board also had built-in random access memory that was accessible by the Xilinx FPGAs.

16. Our WILDSTAR board was installed in a standard Intel-based, x86 host workstation that was located in the RPL at Northeastern University. The workstation's CPU was a commercially available Intel Pentium III processor. The workstation contained at most 4 floating-point multiplier arithmetic units that could multiply input numbers in the 32-bit IEEE single precision format.

17. We tested implementations of complete adder and multiplier circuits that processed various different floating-point formats to determine how many of each could be implemented on a Virtex XCV1000 FPGA on the WILDSTAR board. This included formats that used both more and fewer fraction bits than standard IEEE single-precision floating point numbers (and were, therefore, more or less precise) as well as formats that had more or fewer exponent bits than standard IEEE single-precision floating point numbers (and, therefore, had both wider and narrower dynamic ranges). Specifically, in addition to using a 23-bit fraction and 8-bit exponent, which is the IEEE standard single-precision format, we used a 26-bit fraction with 5-bit exponent and a 20-bit fraction with 11-bit exponent.

18. We also experimented with and tested implementations of adders and multipliers using other formats that used fewer total bits (*i.e.*, 8, 12, 16, and 24 total bits instead of 32 bits). And for those other formats, we used different combinations of exponent and fraction bitwidths. One example was a 12-bit format that used one sign bit, 6 fraction bits, and 5 exponent bits—this is a format we used for some related K-means clustering analyses on the satellite imagery and other data from LANL. Another example was a 16-bit format that used one sign bit, 9 fraction bits, and 6 exponent bits.

19. We synthesized adders and multipliers using formats with a variety of these combinations onto the Xilinx XCV1000 FPGA in an effort to determine how many such multipliers could be put in parallel. Our work showed that 81 complete adder circuits or 61 complete multiplier circuits that processed inputs in the 16-bit format with one sign bit, 9 fraction bits, and 6 exponent bits could fit on a single one of the three Xilinx XCV1000 FPGAs on the WILDSTAR board (and, by extension, that well over 100 of these complete multiplier circuits or complete adder circuits could fit on the WILDSTAR boards' three Xilinx XCV1000 FPGAs). By way of comparison, our work showed that, when using IEEE single-precision formats (*i.e.*, one sign bit, 8 exponent bits, and 23 fraction bits), we could fit only 31 complete adder circuits or 13 complete multiplier circuits onto the same Xilinx XCV1000 FPGA.

20. In addition to actually synthesizing and loading large sets of floating-point arithmetic operators using different floating-point formats onto FPGAs in our lab (including the 1-6-9 format discussed above), I and others presented VFLOAT and our related work through various presentations, conferences, workshops, meetings, and the like, as well as prepared, distributed, and published written works that described various aspects of VFLOAT and our work related to VFLOAT.

21. For example, in May 2002, Mr. Belanović gave an oral presentation in connection with defending his master's thesis, which was titled "Library of Parameterized Modules for Floating-Point Arithmetic with An Example Application." Specifically, Mr. Belanović's thesis defense took place in a presentation on Wednesday, May 8, 2002, on the Northeastern University campus in Boston, Massachusetts. Mr. Belanović's presentation to the thesis committee was public, and he was later awarded his M.S. degree in Electrical Engineering from the Northeastern University Department of Electrical and Computer Engineering on the basis of the presentation and underlying work. During his thesis defense, Mr. Belanović orally presented on various aspects of VFLOAT and our work related to VFLOAT, including displaying and discussing our conclusions regarding the maximum number of complete VFLOAT floating-point addition and multiplication operators that could in practice be mapped to each of the three Xilinx XCV1000 FPGAs on our WILDSTAR board.

22. Other members of the Northeastern University community also learned of and became familiar with VFLOAT during the time it was being developed and in subsequent years after it was made publicly available, including for example the graduate students who contributed to later iterations or revisions of VFLOAT over the years (*e.g.*, Haiqian Yu in 2003 and Xiaojun Wang in 2008) as well as several other graduate students whom I supervised, including Shawn Miller, Joshua Noseworthy, Albert A. Conti III, and Ben Cordes. The RPL lab itself, where the physical workstation described above was located, was a shared space in which, at any given time, at least a dozen and possibly as many as 20 other students and faculty members within the Department of Electrical and Computer Engineering routinely worked and to which they had unrestricted access. In addition, I specifically recall demonstrating VFLOAT and our physical workstation that included the WILDSTAR reconfigurable computing engine in

approximately 2002 to Laurie Smith King, a Professor of Computer Science at Holy Cross University, who spent a sabbatical at Northeastern University during that timeframe.

23. During my secondary appointment as a Visiting Scientist at MIT's Lincoln Laboratories from June to December 2002, I attended and presented at the Sixth Annual Workshop on High Performance Embedded Computing (HPEC 2002), which was held at the MIT Lincoln Laboratory from September 24-26, 2002. Approximately 100 individuals attended HPEC 2002 overall, and approximately 30-40 individuals attended the session in which I presented various aspects of VFLOAT. In my forthcoming report, I intend to discuss how my presentation at HPEC 2002, among other public disclosures, supports an opinion regarding the invalidity of the Asserted Claims.

24. Among other things, I disclosed at HPEC 2002 that our system setup used a WILDSTAR reconfigurable computing engine from Annapolis Micro and that the WILDSTAR board had three Xilinx Virtex XCV1000 FPGAs as well as memory; the various modules that comprised the VFLOAT library and how they could be used to assemble floating-point arithmetic units such as adders and multipliers; our synthesis results and conclusions regarding the size of VFLOAT arithmetic modules when mapped to FPGA hardware; and how many complete arithmetic circuits would fit on the hardware we used—specifically, our results showed that 85 multipliers using a 12-bit format could fit on a single Xilinx XCV1000 FPGA whereas only 13 multipliers could fit on the same FPGA if using IEEE single-precision format (with 32 bits).

25. At the HPEC conference in 2002, I also discussed how 16-bit formats would allow one to fit over 75 complete adder circuits or over 50 complete multiplier circuits onto a single one of the three Xilinx Virtex XCV1000 FPGAs on a WILDSTAR board. At a high level,

the presentation emphasized the tradeoffs between area and power, on the one hand, and precision and dynamic range, on the other, as well as the fact that using smaller bitwidths allowed one to get more parallelism for increased speed.

26. In my forthcoming report, I intend to explain how my work related to VFLOAT, and related public disclosures at conferences, workshops, meetings, and the like, invalidates the Asserted Claims. In particular, I plan to address how the public knowledge about VFLOAT and our implementation and public use of VFLOAT using formats such as the one with 6 exponent bits and 9 fraction bits meets the limitations of the Asserted Claims.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct to the best of my knowledge.

Executed on December 9, 2022, at Boston, Massachusetts.

DocuSigned by:
Miriam Leeser
6014FF41805C4EA...

Miriam Leeser